IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re US Appln. of : Kazuya ONO

U.S. Application Serial No. 09/973,795 Filed: October 11, 2001

Japanese Patent Appln. No.: 2000-310113

Japanese Patent Application Filing Date : October 11, 2000

For : Serial Communication Device and Method of Carrying out Serial Communication

Art Unit: 2113 Confirmation No. 7244

Examiner: Maskulinski, Michael C Attorney Docket No.: A319-1

MAIL STOP AMENDMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

VERIFICATION OF TRANSLATION OF PRIORITY DOCUMENT

Dear Sir:

The undersigned hereby declares:

(1) that I am conversant in both the Japanese and English languages;

(2) that I have prepared the attached English translation of Japanese Patent Application No. 2000-310113, filed October 11, 2000;

(3) that the English translation is a true, faithful and accurate translation of the above-identified Japanese Application to the best of my knowledge and belief; and

(4) that all statements made of my own knowledge are true and that all statements made on information and belief are with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC § 1001, and that such false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date June 13, 2006

Signature 

Typed Name: HIROSHI AMANO

Address: Sine-Mita Bldg. 5F, 40-4, Shiba 3-chome, Minato-ku, Tokyo, Japan

Attachment:

English translation of Japanese Patent Application No. 2000-310113

[Document Name] Patent Application

[File Reference] 40410514

[Filing Date] October 11, 2000

[Address] Commissioner, Patent Office

[International Patent Classification] H04L 29/08

[Inventor]

[Address] c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo

[Name] Kazuya ONO

[Applicant]

[Identification Number] 000004237

[Name] NEC Corporation

[Agent]

[Identification Number] 100097113

[Patent Attorney]

[Name] Shiroyuki HORI

[Indication of Fee]

[Prepayment Ledger Number] 044587

[Amount of Payment] ¥21,000

[List of Attachment]

[Name of Attachment] Specification 1

[Name of Attachment] Set of Drawings 1

[Name of Attachment] Abstract 1

[Number of General Power of Attorney] 9708414

[Necessity of Proof] Necessary

[Document Name] Specification

[Title of the Invention] Serial Communication Device and Method of carrying out Serial Communication

[Claims]

[Claim 1] A serial communication device providing bus-bridge between a parallel bus and a serial bus, comprising:

a parallel-serial converter which converts parallel data output through said parallel bus, into serial data; and

a check bit producer which applies an error correcting code to said serial data converted by said parallel-serial converter.

[Claim 2] The serial communication device as set forth in claim 1, further comprising a parallel bus interface which multiplexes said parallel data transmitted through said parallel bus, into predetermined bits, and outputs the thus multiplexed parallel data to said parallel-serial converter,

and wherein said parallel-serial converter converts said parallel data into serial data every said predetermined bits, and

said check bit producer applies said error correcting code to every said predetermined bits of said serial data converted by said parallel-serial converter.

[Claim 3] A serial communication device providing bus-bridge between a parallel bus and a serial bus, comprising:

a serial-parallel converter which converts serial data output through said serial bus, into parallel data; and

an error detector which checks an error correcting code applied to said serial data to thereby detect an error when said serial data is converted into said parallel data by said serial-parallel converter.

[Claim 4] The serial communication device as set forth in claim 3, further comprising an error corrector which corrects an error detected in said error correcting code by said error detector.

[Claim 5] The serial communication device as set forth in claim 3 or 4,

wherein said error corrector corrects said error when said error detected by said error detector in said error correcting code is a 1-bit error, and abandons an associated access when said error detected by said error detector in said error correcting code is a 2-bit error.

[Claim 6] A serial communication device providing bus-bridge between a parallel bus and a serial bus, comprising:

a parallel-serial converter which converts parallel data output through said parallel bus, into serial data;

a check bit producer which applies an error correcting code to said serial data converted by said parallel-serial converter;

a serial-parallel converter which converts serial data output through said serial bus, into parallel data; and

an error detector which checks said error correcting code applied to said serial data to thereby detect an error when said serial data is converted into said parallel data by said serial-parallel converter.

[Claim 7] A method of carrying out serial communication for providing bus-bridge between a parallel bus and a serial bus, comprising:

converting parallel data output through said parallel bus, into serial data; and

applying an error correcting code to the thus converted serial data.

[Claim 8] The method as set forth in claim 7, further comprising:

multiplexing said parallel data transmitted through said parallel bus, into predetermined bits;

converting said parallel data into serial data every said predetermined bits, and

applying said error correcting code to every said predetermined bits of the thus converted serial data.

[Claim 9] A serial communication device providing bus-bridge between a parallel bus and a serial bus, comprising:

converting serial data output through said serial bus, into parallel data; and

checking an error correcting code applied to said serial data to thereby detect an error when said serial data is converted into said parallel data.

[Claim 10] The method as set forth in claim 9, wherein an error is corrected when said error is detected in said error correcting code.

[Claim 11] The method as set forth in claim 9 or 10, wherein said error detected in said error correcting code is corrected when said error is a 1-bit error, and an associated access is abandoned when said error detected in said error correcting code is a 2-bit error.

[Claim 12] A method of carrying out serial communication for providing bus-bridge between a parallel bus and a serial bus, comprising:

converting parallel data output through said parallel bus, into serial data;

applying an error correcting code to the thus converted serial data;

converting serial data output through said serial bus, into parallel data; and

checking an error correcting code applied to said serial data to thereby detect an error when said serial data is converted into said parallel data.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The invention relates to a serial communication device and a method of carrying out serial communication both used for confounding a memory in duplex in a system for duplexing a processor, and more particularly to such a serial communication device and a method of carrying out serial communication both presenting the same reliability as reliability presented by a parallel bus.

[0002]

[Prior Art]

FIG. 3 is a block diagram of a conventional system for making communication in duplex confounding.

Conventional communication in duplex confounding is made through a

32-bit address bus 13 and a 32-bit data bus 14 both extending between a parallel bus controller 10 and another parallel bus controller 12.

[0003]

Errors in parallel buses, that is, the 32-bit address bus 13 and the 32-bit data bus 14 are generally detected through a 5-bit parity 15 disposed between the parallel bus controller 10 and the parallel bus controller 12.

[0004]

[Problems to be solved by the Invention]

The conventional system is accompanied with a problem that since the system has to include a lot of signal line for the parallel buses, the system unavoidably has a plurality of buffer circuits 11, resulting in much possibility of defectiveness in fabrication of the system, and high cost for fabricating the system.

[0005]

It would be possible to accomplish reduction in both cost and defectiveness in fabrication of the system, if the parallel buses are replaced with serial buses. However, the use of serial bus causes another problem that bit errors occur during communication, and hence, it is impossible to ensure the same reliability as reliability obtained when parallel buses are used.

[0006]

In view of the above-mentioned problems in the conventional system, it is an object of the present invention to provide a serial communication device and a method of carrying out serial communication both of which are capable of reducing the number of parts by using a serial bus in duplex confounding to thereby accomplish reduction in cost and defectiveness in fabrication, and providing the same reliability as reliability obtained when parallel buses are used, even though serial buses are used.

[0007]

[Solution to the problems]

In order to solve the above-mentioned problems, the invention is presented as follows.

There is provided in claim 1 a serial communication device providing bus-bridge between a parallel bus and a serial bus, including a parallel-serial converter which converts parallel data output through the parallel bus, into serial data, and a check bit producer which applies an error correcting code to the serial data converted by the parallel-serial converter.

There is provided in claim 2 the serial communication device as set forth in claim 1, further including a parallel bus interface which multiplexes the parallel data transmitted through the parallel bus, into predetermined bits, and outputs the thus multiplexed parallel data to the parallel-serial converter, and wherein the parallel-serial converter converts the parallel data into serial data every the predetermined bits, and the check bit producer applies the error correcting code to every the predetermined bits of the serial data converted by the parallel-serial converter.

There is provided in claim 3 a serial communication device providing bus-bridge between a parallel bus and a serial bus, including a serial-parallel converter which converts serial data output through the serial bus, into parallel data, and an error detector which checks an error correcting code applied to the serial data to thereby detect an error when the serial data is converted into the parallel data by the serial-parallel converter.

There is provided in claim 4 the serial communication device as set forth in claim 3, further including an error corrector which corrects an error detected in the error correcting code by the error detector.

There is provided in claim 5 the serial communication device as set forth in claim 3 or 4, wherein the error corrector corrects the error when the error detected by the error detector in the error correcting code is a 1-bit error, and abandons an associated access when the error detected by the error detector in the error correcting code is a 2-bit error.

There is provided in claim 6 a serial communication device providing bus-bridge between a parallel bus and a serial bus, including a parallel-serial converter which converts parallel data output through the parallel bus, into serial data, a check bit producer which applies an error correcting code to the serial data converted by the parallel-serial converter, a serial-parallel converter which converts serial data output through the serial bus, into parallel data, and an error detector which checks the error correcting code applied to the serial data to thereby detect an error when the serial data is converted into the parallel data by the serial-parallel converter.

There is provided in claim 7 a method of carrying out serial communication for providing bus-bridge between a parallel bus and a serial bus, including converting parallel data output through the parallel bus, into serial data, and applying an error correcting code to the thus converted serial data.

There is provided in claim 8 the method as set forth in claim 7, further including multiplexing the parallel data transmitted through the parallel bus, into predetermined bits, converting the parallel data into serial data every the predetermined bits, and applying the error correcting code to every the predetermined bits of the thus converted serial data.

There is provided in claim 9 a serial communication device providing bus-bridge between a parallel bus and a serial bus, including converting serial data output through the serial bus, into parallel data, and checking an error correcting code applied to the serial data to thereby detect an error when the serial data is converted into the parallel data.

There is provided in claim 10 the method as set forth in claim 9, wherein an error is corrected when the error is detected in the error correcting code.

There is provided in claim 11 the method as set forth in claim 9 or 10, wherein the error detected in the error correcting code is corrected when the error is a 1-bit error, and an associated access is abandoned when the error

detected in the error correcting code is a 2-bit error.

There is provided in claim 12 a method of carrying out serial communication for providing bus-bridge between a parallel bus and a serial bus, including converting parallel data output through the parallel bus, into serial data, applying an error correcting code to the thus converted serial data, converting serial data output through the serial bus, into parallel data, and checking an error correcting code applied to the serial data to thereby detect an error when the serial data is converted into the parallel data.

[0008]

[Embodiments of the Invention]

An embodiment in accordance with the present invention is explained hereinbelow with reference to the drawings.

[0009]

FIG. 1 is a block diagram of the serial communication device in accordance with a preferred embodiment of the present invention.

[0010]

With reference to FIG. 1, the embodiment is comprised of a bus bridge circuit 8 electrically connected to a parallel bus 1 including a 32-bit address bus and a 32-bit data bus, a parallel-serial converting circuit 4 electrically connected between the bus bridge circuit 8 and a serial bus 5, and a serial-parallel converting circuit 6 electrically connected between the bus bridge circuit 8 and the serial bus 5.

[0011]

The bus bridge circuit 8 is comprised of a parallel bus interface circuit 2 electrically connected to the parallel bus 1, a parallel-serial interface circuit 3 electrically connected to the parallel-serial converting circuit 4, a serial-parallel interface circuit 7 electrically connected to the serial-parallel converting circuit 6, and a 8-bit data-multiplexing bus 9 electrically connecting the parallel bus interface circuit 2 to the parallel-serial interface circuit 3 and the serial-parallel

interface circuit 7.

[0012]

The parallel bus interface circuit 2 act as an interface to the parallel bus 1. When data is transmitted to the serial bus 5 from the parallel bus 1, the parallel bus interface circuit 2 multiplexes 32-bit address, data and command transmitted through the parallel bus 1, into 8-bit (1 byte) addresses, data and commands, and outputs the thus multiplexed addresses, data and commands to the parallel-serial interface circuit 3 through the data-multiplexing bus 9. When data is transmitted to the parallel bus 1 from the serial bus 5, the parallel bus interface circuit 2 transmits data multiplexed into 1-byte data, to the parallel bus 1 through the data-multiplexing bus 9 as 32-bit address, data and command.

[0013]

The parallel-serial interface circuit 3 acts as an interface for transmitting serial data, and produces a bit for checking an error correcting code (ECC) in serial communication. The parallel-serial interface circuit 3 receives address, data and command byte by byte from the parallel bus interface circuit 2, produces a ECC check bit on receipt of 1-byte of address, data and command, applies the thus produced ECC check bit to each 1-byte of address, data and command, and outputs each 1-byte of address, data and command with the associated ECC check bit, to the parallel-serial converting circuit 4. Herein, a ECC check bit means a code for correcting an error in the serial communication system.

[0014]

The parallel-serial converting circuit 4 has a function of converting parallel data to serial data, and hence, converts serial data received from the parallel-serial interface circuit 3 byte by byte, into serial data, and outputs the thus converted serial data to the serial bus 5.

[0015]

The serial-parallel converting circuit 6 has a function of converting

serial data to parallel data, and hence, converts serial data received through the serial bus 5 into parallel data byte by byte, and outputs the thus converted parallel data to the serial-parallel interface circuit 7.

[0016]

The serial-parallel interface circuit 7 has a function of detecting a ECC check bit, and acting as an interface for receiving parallel data. The serial-parallel interface circuit 7 checks ECC check bits in address, data and command to thereby detect errors in error correcting codes, and corrects the detected errors. Then, the serial-parallel interface circuit 7 converts 1-byte data transmitted from the serial-parallel converting circuit 6, into 32-bit address, data and command, and multiplexes the 32-bit address, data and command into 8-bit (1 byte) addresses, data and commands, and outputs the thus multiplexed addresses, data and commands to the data-multiplexing bus.

[0017]

The serial-parallel interface circuit 7, after converting serial data into parallel data, checks the ECC check bits in address, data and command to thereby detect errors in the error correcting codes. If the serial-parallel interface circuit 7 detects a 1-bit error in the error correcting codes, the serial-parallel interface circuit 7 corrects the detected 1-bit error, whereas if the serial-parallel interface circuit 7 detects a 2-bit error in the error correcting code, the serial-parallel interface circuit 7 abandons an access associated the detected error.

[0018]

Hereinbelow is explained an operation of the embodiment.

FIG. 2 is a time chart used for explaining an operation of the serial communication device in accordance with the embodiment of the present invention.

[0019]

When data is transmitted to the serial bus 5 from the parallel bus 1,

the parallel bus interface circuit 2 multiplexes 32-bit address, data and command transmitted through the parallel bus 1, into 8-bit addresses, data and commands, and outputs the thus multiplexed addresses, data and commands to the parallel-serial interface circuit 3 through the 8-bit data-multiplexing bus 9.

[0020]

The parallel-serial interface circuit 3 receives address, data and command byte by byte, produces a ECC check bit on receipt of 1-byte of address, data and command, and applies the thus produced ECC check bit to each 1-byte of address, data and command.

[0021]

Each 1-byte of address, data and command to which the ECC check bit was applied was converted into serial data in the parallel-serial converting circuit 4, and then, transmitted to the serial bus 5.

[0022]

When data is transmitted to the parallel bus 1 from the serial bus 5, address, data and command are transmitted to the serial-parallel converting circuit 6 through the serial bus 5, and are converted into parallel data in 1-byte in the serial-parallel converting circuit 6. The thus converted 1-byte parallel data are transmitted to the serial-parallel interface circuit 7.

[0023]

The serial-parallel interface circuit 7 converts the 1-byte serial data transmitted from the serial-parallel converting circuit 6, into 32-bit address, data and command, and multiplexes the 32-bit address, data and command into 8-bit (1 byte) addresses, data and commands, and outputs the thus multiplexed addresses, data and commands through the 8-bit data-multiplexing bus 9.

[0024]

In addition, the serial-parallel interface circuit 7 checks and corrects the ECC check bits applied to address, data and command in 1 byte by virtue of the function of detecting and correcting an ECC check bit. If the serial-parallel

interface circuit 7 detects a 1-bit error in the error correcting codes, the serial-parallel interface circuit 7 corrects the detected 1-bit error. If the serial-parallel interface circuit 7 detects a 2-bit error in the error correcting code, the serial-parallel interface circuit 7 abandons an access associated the detected error.

[0025]

The 32-bit address, data and command are transmitted to the parallel bus interface circuit 2 from the serial-parallel interface circuit 7, and then, transferred to the parallel bus 1.

[0026]

With reference to FIG. 2, the parallel-serial interface circuit 3 produces the ECC check bits for address, data and command, and applies the ECC check bits to each 1-byte of address, data and command at timings illustrated in FIG. 2. Similarly, the serial-parallel interface circuit 7 checks the ECC check bits in address, data and command at timings illustrated in FIG. 2.

[0027]

In accordance with the above-mentioned embodiment, the number of parts for constituting the communication system such as signal lines, bus drivers and bus receivers can be reduced by using a serial bus in duplex confounding to thereby accomplish reduction in cost and defectiveness in fabrication of the communication system, and the same reliability as reliability obtained when parallel buses are used can be provided, even though serial buses are used.

[0028]

The embodiment in accordance with the present invention has the above-mentioned structure. The embodiment can be applied to a parallel bus and a serial bus having any specification.

[0029]

It is to be understood that the subject matter encompassed by way of the present invention is not to be limited to the above-mentioned embodiment.

The embodiment may be changed within the spirit and scope of the present invention. The number, position and shape of the parts constituting the embodiment may be changed into the number, position and shape preferable to put the present invention into practice. In the drawings, parts or elements have been provided with the same reference numerals.

[0030]

[Advantages obtained by the Invention]

The serial communication device and the method of carrying out serial communication both in accordance with the present invention provides an advantage that the number of parts for constituting the communication system such as signal lines, bus drivers and bus receivers can be reduced by using a serial bus in duplex confounding to thereby accomplish reduction in cost and defectiveness in fabrication of the communication system, and the same reliability as reliability obtained when parallel buses are used can be provided, even though serial buses are used.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 is a block diagram of the serial communication device in accordance with the present invention.

[FIG. 2]

FIG. 2 is a time chart showing an operation of the serial communication device in accordance with the present invention.

[FIG. 3]

FIG. 3 is a block diagram of a conventional system for making communication in duplex confounding.

[Indication by Reference Numerals]

1 Parallel bus

2 Parallel bus interface circuit

3 Parallel-serial interface circuit

4 Parallel-serial converting circuit

5 Serial bus

6 Serial-parallel converting circuit

7 Serial-parallel interface circuit

8 Bus bridge circuit

9 Data-multiplexing bus

10 Parallel bus controller

11 Buffer circuit

12 Another parallel bus controller

13 Address bus

14 Data bus

15 Parity

[Title of Document] Abstract

[Abstract]

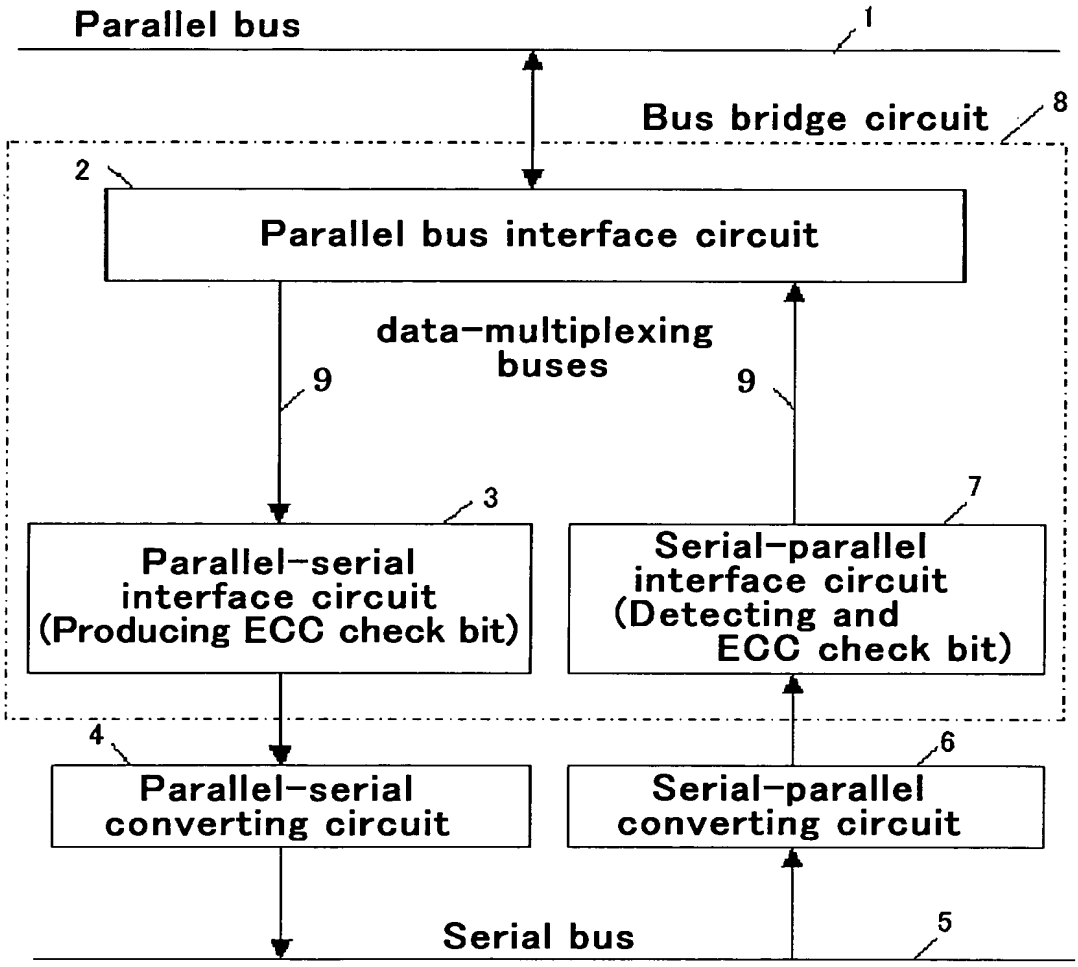
[Object] To provide a serial communication device and a method of carrying out serial communication both of which are capable of providing the same reliability as reliability obtained when parallel buses are used, even though serial buses are used.

[Solution] The parallel-serial interface circuit 3 acts as an interface for transmitting serial data, and produces a bit for checking an error correcting code (ECC) in serial communication. The parallel-serial interface circuit 3 produces a ECC check bit on receipt of 1-byte of address, data and command, applies the thus produced ECC check bit to each 1-byte of address, data and command, and outputs the address, data and command to the parallel-serial converting circuit 4. The serial-parallel interface circuit 7 has a function of detecting and correcting a ECC check bit, and acting as an interface for receiving parallel data. The serial-parallel interface circuit 7 checks ECC check bits in address, data and command to thereby detect errors in error correcting codes, and corrects the detected errors.

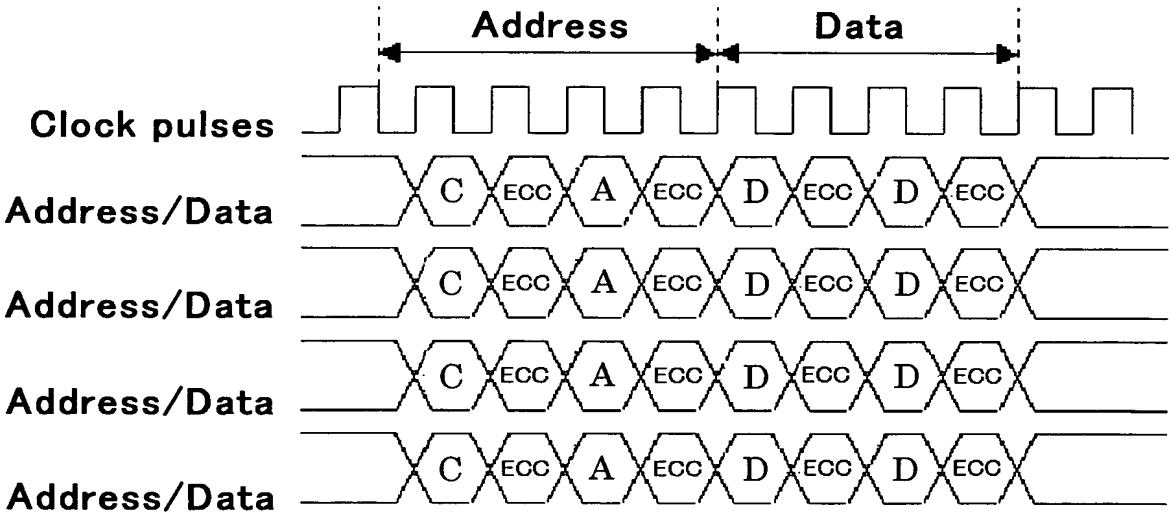
[Representative Drawing] FIG. 1

【Title of Document】 Drawings

【Fig.1】



【Fig.2】



C : COMMAND
A : ADRESS
D : DATA

【Fig.3】